# Course: Very Deep Submicron Layout (VDSL)

## Course Code
VDSL01

## Course Pre-requisite
Prior experience of analog layout on a CMOS process

## Learning Outcomes
- Layout of VDSL circuits on CMOS processes
- Understanding the impact layout has on yield and discuss how yield is no longer just a foundry responsibility
- Understanding the parasitics elements introduced by the VDSL process

## Syllabus Content – Summary
- CMOS Scaling Implications
- Yield
- Interconnect Parasitics
- Device Parasitics
- Matching
- Isolation Strategies
- Design for Manufacture

## Syllabus Content – Detailed
**CMOS Scaling**
Overview of the implications on layout of working on VDSM technology nodes.
- Moore's Law
- Scaling Challenges
- CMOS Scaling Implications
- Shallow Trench Isolation (STI)
- Well Proximity Effect (WPE)

**Yield**
Understanding the impact layout has on yield and discusses how yield is no longer just a foundry responsibility.
- Key Factors
- Lithography
- Optical Proximity Correction (OPC)
- Phase Shift Mask (PSM
- Chemical Mechanical Polishing (CMP)

**Interconnect Parasitics**
Introduces the parasitic elements introduced by the layout process during interconnect.
- Resistance
- Capacitances
- Extractions

**Device Parasitics**
An examination of the layout techniques used for laying out MOS transistors and other CMOS components so as to reduce power consumption, reduce area and increase frequency of operation.
- Resistor Model
- Capacitor Model
- MOS Model

**Design For Manufacturing (DFM)**
Discussion on a new element in the design flow on VDSM technologies where layouts have to be designed with manufacturing in mind.
- Design Rules
- Layout For High Yield
- Lithography Aware Layout

**More Information:**
http://www.icmaskdesign.com