RF Layout Techniques

Master IC Training™

The RF Physical Design course is targeted towards developing the skills necessary to complete the layout of an RF design. With a primary focus on CMOS processes, the course discusses the many challenges faced by RF CMOS layout and provides practical real life solutions.

COURSE CODE: RFLT01

COURSE PRE-REQUISITE: Prior experience of analog layout on a CMOS process

LEARNING OUTCOMES:

- Layout of RF circuits on CMOS processes
- Understanding of how layout influences circuit performance
- Schematic structure recognition and physical implementation

SYLLABUS CONTENT:

- Parasitics
  - Resistance and capacitance of interconnect
  - Inductance of interconnect
  - Device parasitics
- High speed MOS devices
  - Optimising device parasitics associated with MOS transistors
  - Unit fingers, donut devices, lattice structures
- Matching methodologies
  - Unit fingers, interleaving, common centroid, dummy insertion
- Shielding
  - Methodologies for shielding devices and interconnect from noise sources
- Substrate & Wells
  - Substrate model
  - Noise isolation techniques
  - Latch-up
- Supply considerations in RF designs
  - Isolation (natural decoupling)
  - Matched IR drop
  - Electromigration
- RF Components
  - Inductors
  - Varactor diodes
  - Flux capacitors

Course Delivery:
Lecture and practical labs with example circuits