Layout for ESD

This course focuses on the layout of devices used in ESD protection schemes for ICs. Content includes device compositions, parasitic effects of ESD structures, isolation schemes, and whole chip ESD protection methodologies.

COURSE CODE: ESDLT01

COURSE PRE-REQUISITE: None

LEARNING OUTCOMES

- A basic understanding of ESD Protection methodologies
- Understanding the parasitic elements introduced by ESD structures
- Understanding the layout of ESD protection devices

SYLLABUS CONTENT

- ESD Defined
  - Introduction to ESD
  - ESD protection schemes
  - ESD related failures
- CMOS Technology Review
- Diode ESD protection device
- Resistor ESD protection device
- MOS ESD protection device
- Ground/Power Strategies
- Design Rules specific to ESD
  - Electromigration issues (i.e. spacings, thickness, uniform current densities, etc.)
- RF/Mixed Signal ESD Protection Schemes
  - Parasitic effects of ESD protection structures
  - Noise Isolation
- Whole Chip ESD Protection Schemes
  - Input ESD Protection Schemes
  - Output ESD Protection Schemes
  - Power Clamps
  - Multiple domains

COURSE DELIVERY

2-day lecture

MORE INFORMATION

http://www.icmaskdesign.com