ICmask design

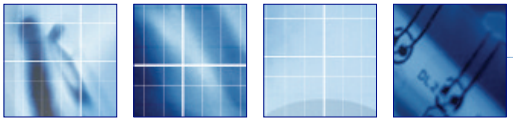
Complete Physical Design Services • IC Layout • Training

ABOUT IC MASK DESIGN

IC Mask Design is an industry leader in the provision of Physical Design Services to the semiconductor industry. Our services encompass IC Layout and Training Programs.

IC Mask Design delivers expertise in analog, RF, mixed-signal and digital design using the latest tools from leading EDA vendors. We also provide training courses covering the complete spectrum of physical design.

Confidence in our technical ability and course delivery is evident, with a number of Fortune 500 semiconductor companies retaining our services. Our extensive expertise and proven track record makes IC Mask Design the partner of choice for leading semiconductor organisations.



MISSION STATEMENT

"To build a high value company which delivers physical design services (implementation and training) of exceptional quality to the global semiconductor industry."

Why engage with IC Mask Design?

TECHNICAL

Experienced IC Layout team

Focus on quality

Delivers within schedule

Familiarity with all major toolset flows

Demonstrated ability to implement complex designs

BUSINESS

Customer focused strategy

Established company with world wide customer base

Proven track record with Fortune 500 companies

Customer confidence on delivery

IC Layout Services

- Full Custom Analog Layout
- RF Layout
- Standard Cell Place & Route / SOC Deployment

FULL CUSTOM ANALOG LAYOUT

Decreasing geometries with increasing frequencies has a greater effect on silicon performance along with increasing the complexity of analog layout. Our analog physical design team ensures our customers receive the highest quality deliverables, on schedule.

The IC Mask Design Advantage

- Experience of taping out to multiple foundries across a broad range of processes
- Proven track record of high quality deliverables on schedule
- Completed multiple design types for a leading world wide customer base
  - Data converters
  - High speed serial communications
  - Clock synthesizers/recovery
  - Storage read/write channels

Flexibility

- IC Mask Design works as an extension of customers own design team
- Design services can be carried out either off-site or on-site depending on customers specific requirements

'IC Mask Design were flexible and delivered on time within the design constraints imposed'

RF LAYOUT

IC Mask Design has a proven world-class RF physical design team with expertise across a broad spectrum of designs and processes, including RF CMOS. We offer our customers an outsourcing team that understands the issues and challenges associated with high frequency physical design.

The IC Mask Design Advantage

- Completed designs in production:
  - Wireless communications
  - GSM/GPRS/3G Applications
  - Fibre-optics
- RF physical design team that has worked with leading Fortune 500 companies worldwide
- Completed layout for designs operating up to 10GHZ
  - Voltage Controlled Oscillators
  - Low Noise Amplifiers
  - Data Serialisers
  - Frequency Mixers

Flexibility

- Experienced team with multiple RF design tape outs

'IC Mask Design have two key qualities ... their very experienced engineering team ... their flexibility and commitment'

PLACE & ROUTE

At IC Mask Design, our physical design team has extensive place and route expertise, addressing the complete design spectrum from RTL through to GDSII.

Our place and route services, including synthesis, timing closure and static timing analysis, provides our customers with a one-stop solution for all their digital layout requirements.

'The next time we have a similar need, IC Mask Design will certainly be our first port of call'

What distinguishes us from our competitors

- Experience taping out designs using the latest tools from all the leading EDA vendors
- Ability to rapidly adopt and integrate new tools and flows
  - Minimal ramp up time
- Streamlined design flow to reduce project time scales without compromise on quality
- Customer confidence that final delivery matches initial specification
  - Detailed program management
  - Milestone deliveries

Engagement options

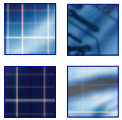
- One-stop solution for all place and route requirements
  - RTL to GDSII
  - Large scale SOC
  - Full turn-key solution
  - IP Hardening

MASTER-IC™ - Physical Design Training Programs

MASTER-IC™ - is a comprehensive Physical Design Training Program, targeted at all levels of expertise, that focus on the development of physical design skills, and are independent of any EDA tool environment

Master IC Training™ includes the following training programs:

- Layout Basics
- Analog Layout Techniques
- Analog Layout, Advanced Techniques
- RF Physical Design
- Custom Digital Layout Techniques
- Standard Cell Place and Route
- Timing Closure in the Backend Flow



COURSE TITLE: Layout Basics

The Layout Basics course introduces the knowledge and skills required to complete the full custom layout of a CMOS design, including the floorplanning, implementation and physical verification stages.

COURSE CODE: LBT01

COURSE PRE-REQUISITE: None

LEARNING OUTCOMES:

1. Familiarity with CMOS logic processes
2. Familiarity with layout interconnect principles and techniques
3. Have a basic understanding of physical design methodologies

SYLLABUS CONTENT:

CMOS technologies and processing layers
MOS transistor layout
Silicon area reduction techniques
Connection techniques
Floorplanning
Physical design methodologies

Course Delivery:
Lecture and practical labs with example circuits

COURSE TITLE: Analog Layout Techniques

The Analog Layout Techniques course provides an introduction to the area of full custom analog layout. Focusing primarily on mixed mode CMOS processes, the course teaches the techniques used in producing high quality layouts of base band analog designs.

COURSE CODE: ANLT01

COURSE PRE-REQUISITE: None

LEARNING OUTCOMES:

1 Familiarity with mixed mode CMOS and BiCMOS processes

2 Understand the layout techniques for resistors & capacitors

3 Knowledge of floorplanning methodologies

4 Ability to layout analog designs on mixed mode CMOS processes

SYLLABUS CONTENT:

Mixed mode CMOS process overview
BiCMOS process
MOS transistor layout
CMOS components used in analog design
Common analog layout techniques
Floorplanning
Power routing techniques

Course Delivery:
Lecture and practical labs with example circuits

COURSE TITLE: Analog Layout, Advanced Techniques

The Analog Layout, Advanced Techniques course aims to further develop the physical design skills of the analog layout engineer, by covering the techniques necessary to produce high quality, well matched and noise tolerant layouts of challenging designs on both CMOS and BiCMOS processes.

COURSE CODE: AALT01

COURSE PRE-REQUISITE:
Prior experience of analog layout on CMOS processes

LEARNING OUTCOMES:

1. Layout of complex analog circuits
2. Matching and noise tolerant analog techniques
3. Schematic structure recognition and physical implementation

SYLLABUS CONTENT:

Device matching in analog circuits
Layout techniques used in low noise applications
Parasitics
Shielding
Schematic structure recognition
Power routing techniques
Bipolar devices in a BiCMOS process

Course Delivery:
Lecture and practical labs with example circuits

COURSE TITLE: RF Physical Design

The RF Physical Design course is targeted towards developing the skills necessary to complete the layout of an RF design. With a primary focus on CMOS processes, the course discusses the many challenges faced by RF CMOS layout and provides practical real life solutions.

COURSE CODE: RFLT01

COURSE PRE-REQUISITE:
Prior experience of analog layout on CMOS processes

LEARNING OUTCOMES:

1. Layout of RF circuits on CMOS processes
2. Understanding of how layout influences circuit functionality
3. Schematic structure recognition and physical implementation

SYLLABUS CONTENT:

Layout factors influencing circuit functionality
MOS transistors at RF
RF Components
Device matching in RF circuits
Power routing techniques
Noise considerations in RF layout
Common RF circuits

Course Delivery:
Lecture and practical labs with example circuits

COURSE TITLE: Custom Digital Layout Techniques

The Custom Digital layout Techniques course focuses on techniques used in the physical design of standard cells, and full custom digital blocks. Starting with the layout of basic MOS transistors, the course develops to cover the more advanced techniques used in creating area efficient full custom digital layouts.

COURSE CODE: CDLT01

COURSE PRE-REQUISITE: None

LEARNING OUTCOMES:

1. Familiarity with the concepts of CMOS logic processes
2. Layout of digital cells
3. Silicon area reduction techniques
4. Understanding of custom digital floorplanning methodologies

SYLLABUS CONTENT:

CMOS Logic process overview
MOS transistor layout
Silicon area reduction techniques
Floorplanning methodologies and techniques
Common custom digital layout techniques
Power routing strategies

Course Delivery:
Lecture and practical labs with example circuits

COURSE TITLE: Standard Cell Place and Route

The Standard Cell Place and Route course is ideally suited to both front-end digital designers and physical designers alike. The courses starts by introducing the complete digital design flow from RTL through to GDSII, before focusing on the primary design steps involved in the back-end flow.

COURSE CODE: SCPR01

COURSE PRE-REQUISITE: None

LEARNING OUTCOMES:

1 Basic understanding of digital design flow (RTL to GDSII)

2 Detailed understanding of the standard cell place & route process

3 Ability to place and route a small design

SYLLABUS CONTENT:

Design flow (RTL to GDSII)
Synthesis and gate-level netlists
Layout libraries
Floorplanning
Power routing
Cell placement
Routing

Course Delivery:
Lecture and practical labs with example circuits

COURSE TITLE: Timing Closure in the Backend Flow

The Timing Closure in the Backend Design Flow course develops the skills of place and route engineers by introducing the concepts behind timing analysis and timing closure. It focuses on the common methodologies used to fix all timing violations during the layout process.

COURSE CODE: BETC01

COURSE PRE-REQUISITE:
Prior experience of place and route methodologies

LEARNING OUTCOMES:

1 Understanding of static timing analysis

2 Understanding of challenges faced in achieving timing closure

3 Place & route a digital design including timing closure

SYLLABUS CONTENT:

Static timing analysis
Constraints for layout
Clocking methodologies
Timing driven placement
Placement based optimisation
Physical synthesis
Timing driven routing

Course Delivery:
Lecture and practical labs with example circuits

ENGINEERING STRENGTHS

Industry Experience

100+ Full Chip tape outs, geometries down to 70nm
Pure play foundries and customer specific - CMOS, BiCMOS, SiGe, and SOI

EDA Environments

Extensive experience with the industry leading and emerging technologies
Flow development / optimisation / customisation
Rapid adoption / integration of new tools, minimal ramp-up time

Project Management

Detailed project plans with agreed milestones and delivery dates
Regular updates through scheduled conference calls
Proven multi-site program management

"We had a difficult challenge, designing precision analog circuits in 90nm technology to reside on a baseband processor, in a compressed timescale. IC Mask Design were able to help meet our timescale. They were flexible, and delivered on time within the design constraints imposed. They operated like an extension of our own design team."

Motorola, Ireland.

"IC Mask Design have two key qualities which distinguishes them from other semiconductor physical design houses. The first is their very experienced engineering team which worked extremely fast whilst still producing high quality layout work. The second is their flexibility and commitment. On short notice they were able to assign extra resources at critical times in the project, and the team worked extremely hard to ensure that we taped out on time."

Centillium Communications, France.

Customer Testimonials

"The course content was very comprehensive, abundant and the presentation could not have been better. There was plenty of time for Q & A. Everything was explained as many times as was needed and the course manual was very comprehensive and clear.

We would have no hesitation in recommending this course to anyone interested in ASIC Analog Layout."

PEI-CSRC, Ireland.

"Ceva required a skilled and experienced layout team for a series of complex mixed signal blocks. The challenge was to do this at short notice, on a highly accelerated schedule. IC Mask Design responded superbly, by locating an efficient and experienced team onsite. Over the course of the project, IC Mask Design continued to supply suitable people as needed. Every engineer proved to be flexible, hard working and communicative, integrating seamlessly into the project team. The next time we have a similar need, IC Mask Design will certainly be our first port of call."

Ceva, Ireland.

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