COURSE TITLE: Introduction to CMOS Layout

Master IC Training™

This course introduces the knowledge and skills required to complete the full custom layout of a CMOS design, including the floorplanning, implementation and physical verification stages.

COURSE CODE: ICL01

COURSE PRE-REQUISITE: None

LEARNING OUTCOMES:

- Familiarity with CMOS logic processes
- Familiarity with layout interconnect principles and techniques
- Have a basic understanding of physical design methodologies

SYLLABUS CONTENT:

- Introduction to CMOS processes
  - Basic processing steps (doping, photolithography, etching, deposition)
  - Electrical interaction of layers
  - Fabrication of an inverter
- MOS Transistor layout
  - Basic parameters (channel width & length)
  - Folding transistors / unit fingers
- Substrate & Wells
  - Simple substrate model
  - Soft connects / multiple stamps
  - Latch-up
- Physical Verification
  - DRC / LVS
- Layout of an inverter
  - Methodology for laying out simple CMOS circuits
- Floorplanning
  - Stick diagrams
  - Supply considerations
- Layout of a AND/OR gate
  - Methodology for laying out moderately complex CMOS circuits
- Area reduction techniques
  - Techniques commonly used to reduce silicon area in layouts

Course Delivery:
Lecture and practical labs with example circuits