

The Analog Layout, Advanced Techniques course aims to further develop the physical design skills of the analog layout engineer, by covering the techniques necessary to produce high quality, well matched and noise tolerant layouts of challenging designs on both CMOS and BiCMOS processes.

COURSE CODE: AALT01

COURSE PRE-REQUISITE: Prior experience of analog layout on a CMOS process

LEARNING OUTCOMES:

- Layout of complex analog circuits
- Matching and noise tolerant analog layout techniques
- Schematic structure recognition and physical implementation

SYLLABUS CONTENT:

- Matching methodologies
 - Unit fingers, interleaving, common centroid, dummy insertion
- Analog building blocks
 - Schematic structure recognition and physical implementation of:
 - Current mirrors, differential amplifiers, voltage references
- Parasitics
 - Resistance and capacitance of interconnect
- Shielding
 - Methodologies for shielding devices and interconnect from noise sources
- Substrate & Wells
 - Substrate model
 - Noise isolation techniques
 - Latch-up
- Bipolar considerations
 - Layout considerations for bipolar and BiCMOS circuits
- Supply considerations in analog designs
 - Isolation
 - IR drop
 - Electromigration

Course Delivery:
[Lecture and practical labs with example circuits](#)