

Supplies used in today's ICs vary from about 1V to more than 100V, depending on the technology and the application (flat panel displays, robotics automobile etc.). Also with the advance in shrinking technology nodes and low-power technologies, core voltages are decreasing whilst the interfaces still need to be at the likes of 5V. This high voltage course addresses the key physical design challenges associated with these issues.

COURSE CODE: HVLT01

COURSE PRE-REQUISITE: Experience of analog layout on a CMOS process

LEARNING OUTCOMES

- Knowledgeable of high voltage devices on CMOS processes
- Layout for HV power design
- ESD layout in HV design
- Knowledge of metal routing schemes

SYLLABUS CONTENT

- CMOS fundamentals
 - Overview of how CMOS devices are fabricated
- HV CMOS definition and layout requirements
 - Implications on layout using high operating voltage devices
 - Techniques to allow high voltage operation
 - Different operating levels on one die
 - HV layout for power design
- ESD protection for HV designs
 - Protecting the HV devices from the outside world
- EMI proofing
 - Methods of reducing the effects of EMI on other circuits
- Electromigration and metal routing strategies
 - Layout techniques for improving electromigration resistance and reducing stresses in high current paths

COURSE DELIVERY

2-day lecture

MORE INFORMATION

<http://www.icmaskdesign.com>