

Limerick based IC Mask Design and Tanner EDA Collaborate on Tools to Accelerate Analog Layout Design

IC Mask Design's layout technology and Tanner EDA expertise, to boost IC design productivity and quality worldwide

Moylish Park, Limerick – March 4, 2010 – [IC Mask Design](#), an industry leader in the provision of physical design services to the global semiconductor industry and Tanner EDA, established as a leading tool provider for the design, layout and verification of analog and mixed-signal integrated circuits (ICs), are collaborating on the development of a toolset to accelerate analog layout design. Tanner EDA recognized the value of IC Mask Design's patented layout acceleration platform by exclusively licensing this technology and integrating it into their custom IC design suite. This collaboration with Tanner EDA opens the doors for growth in Asia and US, offering IC Mask Design a faster time to market.

IC Mask Design and Tanner EDA have been [working together since 2007](#). In the course of working with customers to better understand their analog layout design challenges, the partners recognized a need to speed up the analog layout process. In Q2 2010 Tanner EDA will offer a breakthrough toolset based on IC Mask Design's proprietary technology that accelerates and semi-automates physical design activities to improve productivity. The new tool will embed seamlessly into Tanner EDA's powerful and robust layout editor. Designers will be able to automatically generate devices and structures that are silicon-aware and are contextually tuned for their own specific layouts. This new solution gives engineers and managers the benefits of quality and productivity by consistently applying analog layout knowledge and experience to eliminate errors and speed layout cycles.

Commenting on the collaboration, Greg Lebsack, president of Tanner EDA, said, "We are very focused on bringing innovations from trusted, well-regarded partners to our customers, and are pleased to be able to help them benefit from the depth and breadth of IC Mask Design's experience in analog layout design."

Mr. Ciaran Whyte, co-founder and CTO of IC Mask Design, added, "We are pleased to announce this layout acceleration platform, which is recognised by our customers and foundries to significantly accelerate their IC design process, lower design costs, mitigate the risk of costly manufacturing re-spins and ultimately reduce their time to market."

This new product offering compliments IC Mask Design's existing physical design services and methodology focussed IC Layout training courses, as it builds on its reputation for excellence in the IC Layout space worldwide.

Previews of the joint solution developed by IC Mask Design and Tanner EDA will be available from March 9th to March 12th in Booth #12 at the Design Automation & Test in Europe ([DATE](#)) conference in Dresden, Germany.

About IC Mask Design

Founded in 2002, [IC Mask Design](#) is a dynamic engineering organization and industry leader in the provision of Physical Design services to the global semiconductor industry. The company delivers services for analog, RF, mixed-signal and digital designs, and provides a range of training courses covering the complete spectrum of physical design.

About Tanner EDA

[Tanner EDA](#) provides a complete line of [software solutions](#) that catalyze innovation for the design, layout and verification of analog and mixed-signal (A/MS) integrated circuits (ICs). Founded in 1988, Tanner EDA solutions deliver just the right mixture of features, functionality and usability. The company has shipped over 33,000 licenses of its software to more than 5,000 customers in 67 countries.

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