



European Expert Panel Proposes New Analogue IC Design Methodology to Counter the Analogue Bottleneck

<http://www.gsaglobal.org/news/article.asp?article=2010/0630>

San Jose, Calif. (June 30, 2010) – [GSA](#), the voice of the global semiconductor industry, recently hosted a panel of European analogue IC design experts at the GSA & IET International Semiconductor Forum in London on 19 May. The discussion led to a possible solution to the analogue IC design bottleneck. The Global Semiconductor Alliance together with the UK's Institution of Engineering & Technology joined forces to highlight and discuss European trends in semiconductor development. This year's program focused on leveraging and maximising European expertise in analogue/mixed-signal, wireless, low-power applications and quality/reliability to access emerging markets for silicon growth including smart cards, power electronics and home networking.

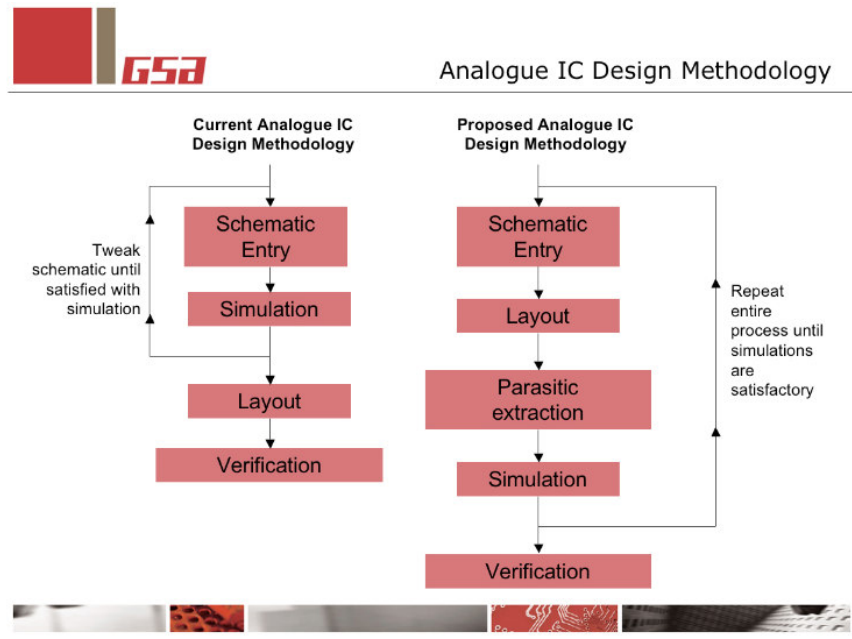
"The panel addressed the problems facing today's analogue designers, including technology and design issues, which are the cause of the analogue bottleneck," explains panel chair Paul Double, GSA's European chair of the Analogue/Mixed-Signal Interest Group and founder and managing director of EDA Solutions Limited. "The discussion resulted in a proposed new methodology for IC design which leads to faster layout, allowing early analysis of the extracted design," added Double.

Market research indicates that although analogue circuitry comprises only 20% of the area in today's modern mixed-signal devices, it is likely to account for some 80% of yield loss. Due to the complexity of the design and dramatic increase in process related design rules to be considered, mixed-signal design, and especially full custom design, is leading to more errors and performance related problems. Manual design and layout is no longer viable, yet automation in the analogue design world remains difficult, and is often an anathema to analogue designers. This quandary is often referred to as the analogue bottleneck.

The findings of the panel discussion suggested a new approach to analogue design to help offset this bottleneck. Because analogue layout at the deeper process nodes is heavily dependent on processing effects, it often does not make sense to perform simulation before the layout stage as in a traditional IC design flow. The solution proposed by the panel to achieve faster layout is to allow early analysis of the extracted design. The flow from schematic to layout has to be accelerated, with simulation only after parasitic extraction. This requires a change in CAD methodology to accelerate the manual layout process.

The existing approach is currently: circuit entry in schematic form, simulation, adjust the schematic, re-simulate, repeat until satisfied with simulation and then on to layout and finally, verification of layout. The new approach proposed by the panel is: schematic, directly to layout, verification including extraction of layout complete with parasitics, simulation, then repeat the entire process until simulations are satisfactory. To support this new methodology, IC design software must feature robust device layout generators, correct by construction placement tools and an integrated router, to enable early analysis and characterisation.

Present on the GSA & IET analogue panel were Ross Addinall, Europe technical director at Ciranova, Peter Frith, chief technical officer of Wolfson Microelectronics, Doug Pattullo, director of Field Technical Support at TSMC Europe and Ciaran Whyte, co-founder and chief technical officer at IC Mask Design. The panel was chaired and moderated by Paul Double, GSA's European chair of the Analogue/Mixed-Signal Interest Group and founder and managing director of EDA Solutions Limited.



Proposed Analogue IC Design Methodology

About GSA: www.gsaglobal.org

The Global Semiconductor Alliance (GSA) mission is to accelerate the growth and increase the return on invested capital of the global semiconductor industry by fostering a more effective fabless ecosystem through collaboration, integration and innovation. It addresses the challenges within the supply chain including IP, EDA/design, wafer manufacturing, test and packaging to enable industry-wide solutions. Providing a platform for meaningful global collaboration, the Alliance identifies and articulates market opportunities, encourages and supports entrepreneurship, and provides members with comprehensive and unique market intelligence. Members include companies throughout the supply chain representing 25 countries across the globe.

About IC Mask Design – www.icmaskdesign.com

IC Mask Design is an industry leader in the provision of Physical Design Services and Software Solutions to the semiconductor industry. The company's services encompass IC Layout and Training Programs, delivering expertise in Analog, RF, mixed-signal and digital design using the latest tools from leading EDA vendors. IC Mask Design also provides training courses covering the complete spectrum of physical design. Its Analog Layout Acceleration Platform aims to dramatically reduce analog layout design cycle time whilst producing optimal quality layout structures which incorporate circuit functionality requirements and process artefacts.

For More Information, Please Contact:

Paul Double, EDA Solutions Limited, Unit A5 Segensworth Business Centre
Segensworth Road, Fareham, PO15 5RQ, UK

Tel: +44 (0) 1489 564253
Fax: +44(0) 1489 557367
E-mail: pauldouble@eda-solutions.com
Web: www.eda-solutions.com

Sally Ward-Foxton, Publitek Limited, 18 Brock Street, Bath, BA1 2LW, UK

Tel: +44 (0) 1225 470000
Fax: +44 (0) 1225 470047
E-mail: sally.ward-foxton@publitek.com
Web: www.publitek.com

Fergal Brosnan, IC Mask Design Limited, EAC, Moylish Park, Limerick, Ireland

Tel: +353 (0)61 448 530
Fax: +353 (0)61 448 531
Email: fbrosnan@icmaskdesign.com
Web: www.icmaskdesign.com