PRODUCT UPDATE

HIGH PERFORMANCE DEVICE GENERATION

New Approach to Accelerating Analog Layout Surpasses Full Custom and Traditional Automation Methodologies

Despite many efforts to automate analog design and layout, these tasks remain primarily a full custom process, with the result that analog is occupying a larger and larger portion of the total design cycle time. Efforts to automate analog design have not been successful in the marketplace because the tools have not been able to equal the quality levels of full custom design, are complex to set up and use, and are expensive.

Tanner EDA's new tool forgoes full automation in favor of accelerating the layout process by generating key analog design primitives, such as current mirrors and differential pairs. These primitives are often the most time–consuming aspect of layout and indeed the parts that are critical to the functionality of the silicon. The new tool applies matching techniques to address common processing artifacts, produces the optimal solution for parasitics and silicon area, and creates devices optimized for high yield.

Layout engineers maintain complete freedom to manually place and route these structures as well as being able to tune the output to their specific requirements. Surpassing traditional automation methodologies, this new layout approach dramatically improves layout productivity and reduces design cycle times while generating structures at a level of quality that consistently matches that of the most experienced layout engineers.

Analog layout is becoming the primary bottleneck in the design process

Analog layout has traditionally been considered to be more challenging than digital layout. For example, it takes considerably more time to achieve a high level of expertise in analog layout as compared to the time required to master digital layout. So it comes as no surprise that digital design automation technology has advanced at a much faster pace than its analog counterpart. Since digital occupies the vast majority of most projects, design cycle times have trended downwards even as transistor counts have continued to increase geometrically.

Right now, most analog layout engineers use either a full custom approach—drawing every polygon—or use basic device generators provided by the foundry to create MOSFETs, capacitors, resistors, etc. The vast majority of layout engineers manually place these devices together to form basic analog structures such as current mirrors and differential pairs, which in turn are connected together to form the overall circuit. The quality of the resulting layout is obviously heavily dependent upon the expertise of the individual layout engineer.

The very long period of time required to develop expertise in analog layout means that skill levels vary widely among the members of the typical layout team. The lack of a consistent approach among members also drives up the time required for the review process and increases the risk of needing additional design spins. These problems appear most often in the more difficult areas of high speed, low noise, high precision analog design where device matching is critical to performance. Expertise even in basic matching techniques can vary from engineer to engineer, which can in some cases lead to the chip failing. Layout engineers with the experience and knowledge to go beyond the basic techniques produce designs that are much more likely to work the first time, but such people are in short supply. A leading analog foundry recently cited matching issues as the single biggest cause of re–spins in their customer's designs.

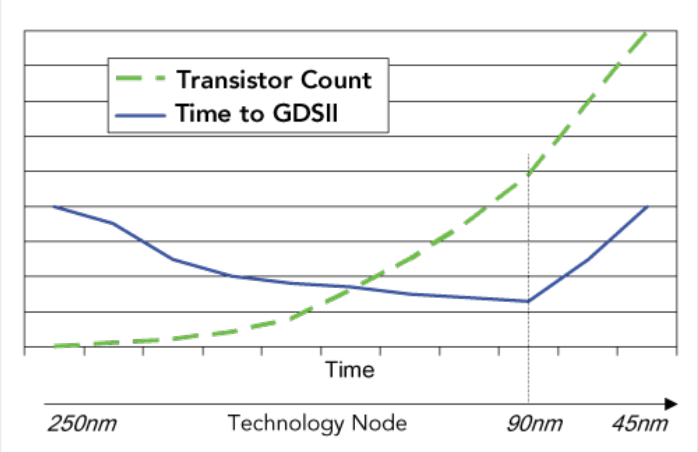

Figure 1: Transistor count vs. time to GDSII by Technology Node

As process technology moves deep into the nanometer realm, the impact of process variations and parasitic effects have caused the analog layout process to be highly iterative and time–consuming. Analog layouts often must be revised, re–simulated and the results evaluated over and over again to achieve a robust solution. In a typical project, analog may occupy only a small portion of the silicon area but can consume a very large portion of the layout effort. As feature sizes are reduced, the time required for full custom analog layout is rising, with the result that many companies are seeing an increase in time–to–GDSII at nanometer technology nodes. Figure 1 shows data collected from a sampling of customers of IC Mask Design, a company that provides analog physical design services.

Existing analog automation solutions have not gained acceptance by users

Large and small vendors offer varying approaches to analog automation, ranging from simple device generation tools to full–blown analog layout automation. One analog automation solution focuses on providing advanced editing features for creating and editing parameterized cells to expedite the process of creating matched structures. Another tool builds on the parameterized cell approach by adding many additional parameters and technology independence. Both operate only at the device level, so they do not address the layout of circuits and structures, which is not only the most time–consuming part of the analog layout process, but also the portion that is most prone to poor quality and inconsistency. Large amounts of time are required to generate individual structures by hand and the quality of the resulting layout varies depending upon the skill of the individual engineer.

Another analog layout solution attempts to completely automate the analog layout process. It provides a programming language that allows users to code their own physical cells and its placement engine generates the layout based on these cells. But the coding takes place at a high level that does not take into consideration the basic characteristics of the key building blocks and may not lay them out with the correct considerations. Users often find that the resulting designs do not compare in quality to a manually created layout. Yet another tool takes as input a set of design rules and then generates basic structures, which are also placed and routed. One weakness of this approach is that it applies global matching rules to the entire layout while skilled manual designers understand that a current mirror, for example, should not be laid out in the same way as a differential pair. One more obstacle to adoption is its list price, which is quoted at close to a million dollars for a single license.

Tanner EDA's HiPer DevGen (High Performance Device Generator) accelerates analog layout by automatically generating common structures

As we've seen above, previous methods to try to automate the analog design process have been primarily based either at the cell level or at the level of the complete design. A new approach is based on accelerating analog layout by generating primitives that are used over and over again such as current mirrors, differential pairs and resistor dividers. This approach creates these building blocks based on an understanding of the functional requirements that are needed to produce a high–quality layout. Rather than attempting to completely automate analog design, HiPer DevGen accelerates the most time–consuming aspects of the layout process to substantially reduce the amount of time required for analog layout while improving quality and design consistency.

By automatically generating the layout of devices—including MOS transistors and resistors as well as MOS current mirrors, MOS differential pairs, resistor dividers and other basic structures—this new approach provides nearly the same degree of acceleration as full automation, but with higher quality. As well as automating the tedious, repetitive aspects of the design process, HiPer DevGen also eliminates the complex and often very expensive setup process that is required with current analog automation tools.

HiPer DevGen automatically generates both devices and analog design primitives using only the manufacturing design rules for the specific technology node as its input. The tool itself understands the technology and matching requirements and automatically generates the basic building blocks of analog layout with these requirements taken into account. Layout engineers have complete freedom to lay out and place and route these structures. HiPer DevGen is provided with basic default values that meet the requirements of 90% of analog designs. For example, in a differential pair it will always attempt to optimize the drain parasitics over the source parasitics. However in circuits such as down mixers, where the source capacitance is more critical, the designer or layout engineer can easily change these parameters, regenerate, simulate the design and converge on an optimal design approach.

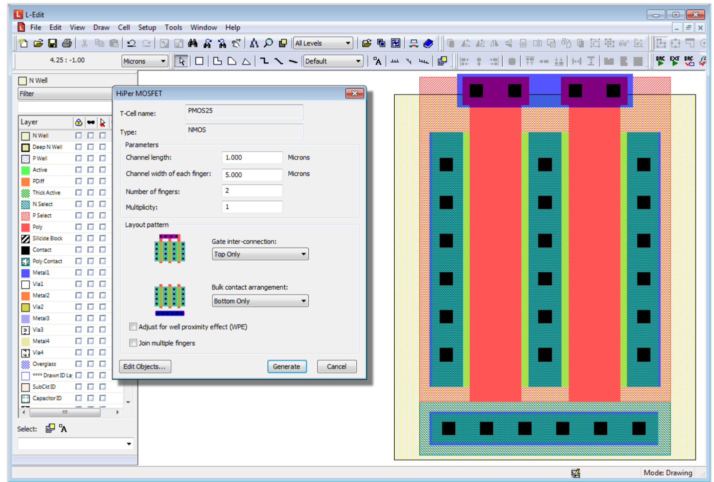

Figure 2: Generation of structures based on existing DRC rules

Retargeting the components to a new technology node simply requires the user to input the manufacturing rules for that technology and regenerate the devices and primitives. So it is possible to very quickly move a design to a new technology node or to a different foundry.

HiPer DevGen was designed to be implemented with little or no change to existing design flows. Unlike existing full automation tools, it works with unmodified schematics. It also uses as input netlists produced for schematic driven layout (SDL) and also accepts input directly from S-Edit, Tanner EDA's schematic editor. HiPer DevGen builds upon Tanner EDA's existing T-Cell architecture of parameterized cells that exist within the company's L-Edit layout editor. The generated cells are cached in the database for maximum performance. HiPer DevGen automatically recognizes the building blocks of the design and generates technology–aware building blocks. The layout engineer then connects the blocks together and wires them to pins to complete the design.

Quality equals that which can be achieved by best analog layout engineers

The HiPer DevGen generation engine is "silicon–aware" and produces devices that are optimized for high yield, including double contacts and vias and support for design for manufacturing (DFM) rules, where applicable. The generation engine takes into account over 20 common processing artifacts and applies matching techniques so that these processing effects are reduced where possible or are applied equally across all matched devices. These artifacts include, but are not limited to:

» Linear process gradients

» Mask misalignment

» Implant shadowing

» Photolithographic invariance

» Current flow direction

» Mechanical stress, including shallow trench isolation (STI) or length of diffusion (LOD)

» Antenna effect/Vt shift

» Well proximity effect (WPE)

HiPer DevGen ensures a consistent and high quality approach to the layout of complex analog structures across layout engineers, design teams and engineering sites. The generation engine considers device and interconnect parasitics and silicon area, and produces the optimal solution based on design inputs, foundry manufacturing rules, and user matching requirements. Matching, parasitic, and performance considerations are tuned to specific analog structures such as the previously mentioned differences between current mirrors and differential pairs. The generation engine understands the key parameters associated with each structure and generates the structures so that these key requirements are met while maintaining a continual focus on silicon quality, yield, silicon performance, and matching.

The generation engine also can be adjusted to ensure that its output fits the user's specific matching, parasitic, and performance requirements. For example, HiPer DevGen offers the user the ability to prioritize parasitic performance over matching requirements or vice versa, and also gives precedence to key matching concerns over others within a circuit. For instance on large devices, where a mismatch due to linear gradients is recognized as being a priority, the generation of the structure can be weighted towards that, as opposed to a possible mismatch in drain or source area.

Examples of how this approach works in practice

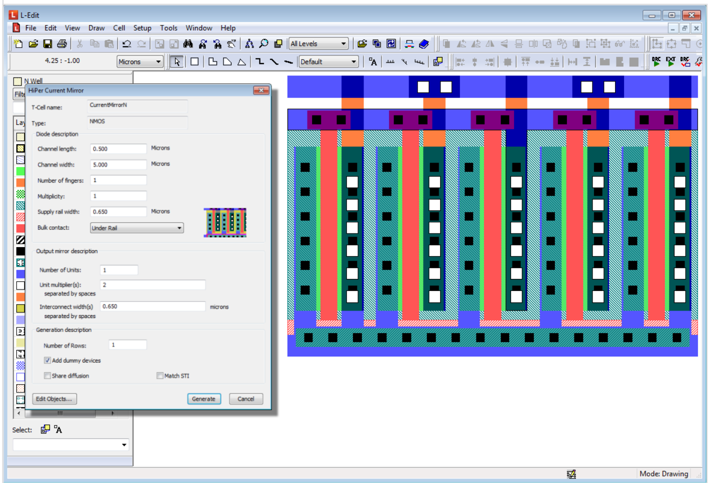

Figure 3: Example current mirror

An example of a current mirror is shown in Figure 3. While an experienced layout engineer would probably spend only a short time to create this structure, the possibility exists that he or she might make an error that could take hours or even days to resolve later in the design cycle. Worse still, such as error could produce a circuit that is LVS and DRC–clean by construction, but has a mismatch, resulting in the problem only being seen in silicon. HiPer DevGen instantly created the structure shown, with the added assurance that it meets all requirements of the targeted technology.

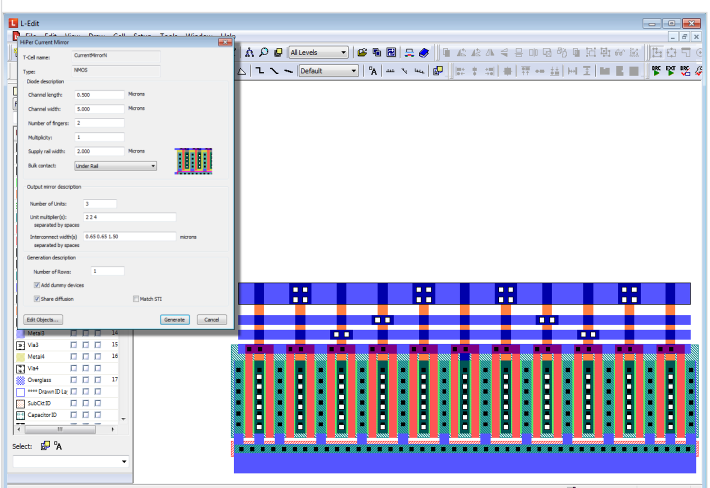

Figure 4: Complex current mirror with dummies

Figure 4 shows a more complex current mirror, again with dummies but in this case there are three output currents. In this case they are being scaled by two, two, and four respectively. This structure would take considerably longer than the first example (Figure 1) if done by hand and its complexity increases the possibility of an error that could cause rework or quality problems. HiPer DevGen also generated this device instantly, with only the manufacturing rules provided as input.

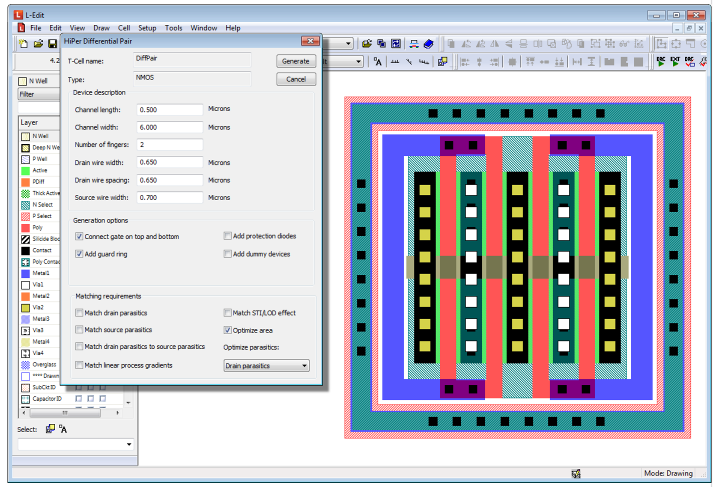

Figure 5: Two finger differential pair.

Figure 5 shows a simple two fingered differential pair with a guard ring. In this case, the drain capacitance is optimized on both devices and the gates are densely connected in metal in order to reduce gate resistance and lower parasitic channel noise. While this example consists of only two transistors with two fingers each, the care required to lay out the structure increases the layout time dramatically. In conjunction with the increased layout effort, the risk of laying it out incorrectly, such as by optimizing the drain, also increases and these errors are typically only spotted either in silicon or where design flows ensure stringent extraction and post–layout simulation of all circuits. With HiPer DevGen, it is possible to create this instantly and, if necessary, generate multiple variants, allowing circuit designers to simulate each solution and converge on an optimal solution for their design in the shortest period of time.

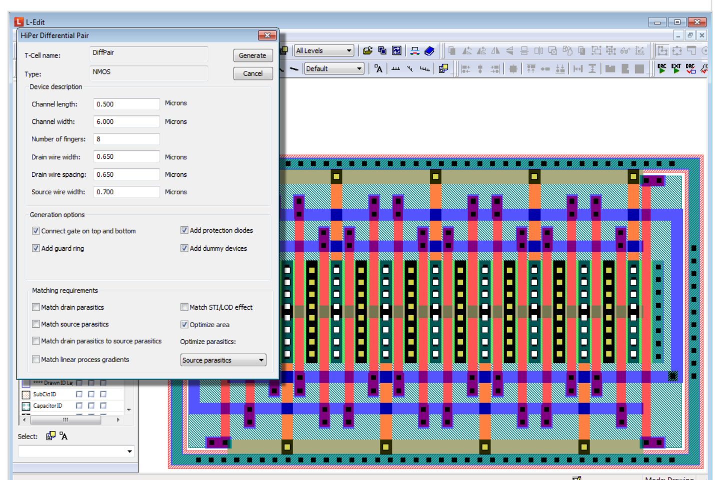

Figure 6: Eight finger differential pair

Figure 6 shows a more complex differential pair with two devices of eight fingers each as well as a guard ring, protection diodes, and dummy devices. In this case, the capacitance of the source also is being optimized. A device of this complexity would take considerably more time than the previous example to lay out by hand. Manual layout would also present considerable risk of error.

For example, moving one of these devices by a micron could introduce a mismatch into the device. HiPer DevGen instantly generated this device while simultaneously providing perfect matching between both devices.

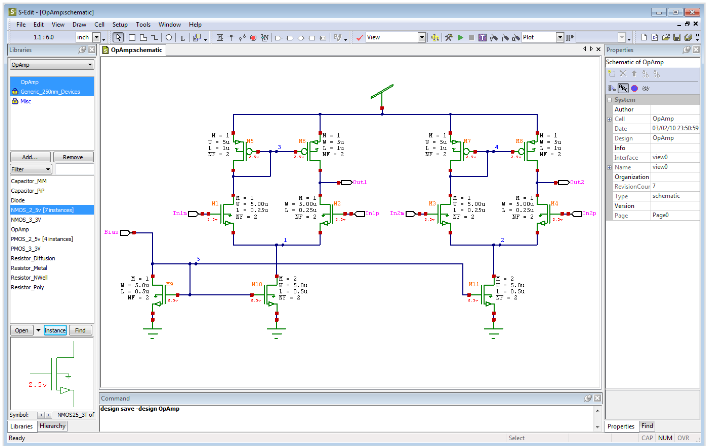

Figure 7: Schematic of example circuit with 17 functional devices

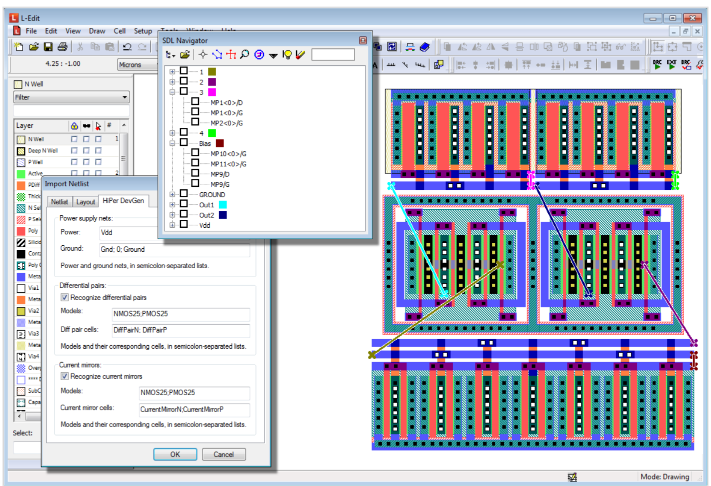

Figure 8: Layout of example circuit with 17 functional devices

Figures 7 & 8 show a complete circuit. The top row of four transistors (two fingers in each device) is made up of two current mirrors, the next row of four transistors (two fingers in each device) is made up of two differential pairs and the bottom row of three transistors is another current mirror, comprising five gates in total. While not shown in the schematic, approximately ten dummy devices would also be required in order to ensure matching, bringing the total device count from seventeen to twenty–seven.

A number of analog layout engineers were asked how long it would take them to lay out this circuit, while obeying best layout practice and applying common matching techniques. Their answers ranged from two hours to two days with an average time of approximately five hours. The complexity of the design means that nearly every engineer would do it differently and these differences have the potential, at best, to lengthen the review process or, at worst, to create yield problems or indeed non–functioning silicon. On the other hand, using HiPer DevGen, a layout engineer instantaneously generated all of the individual structures in the circuit, significantly reducing the overall design effort. The layout engineer then manually floorplanned the circuit and completed the interconnect between devices. Each device or structure was created exactly the same to meet all requirements of the technology, correct by construction in terms of passing layout versus. schematic checks (LVS), DRC clean and with guaranteed matching.

Using this approach, let's suppose that the designer changes a parameter, such as increasing the number of fingers or making the block shorter or wider to fit a different floor plan. Or maybe multiple configurations are required to address parasitics identified during simulation. If the design were done by hand, alternate versions would probably take just as long as the first version to lay out, consuming additional hours or days. With HiPer DevGen, the layout engineer can simply change a parameter and regenerate the structures that make up the design, completing the modifications in a matter of minutes. This acceleration in the design process makes it possible to reduce design cycle time by designing multiple parallel paths to see which one is best for any given circuit. For example, you might evaluate the ability of several different design alternatives to simulate the effects of artifacts such as LOD/STI or WPE.

Conclusion

HiPer DevGen increases analog layout productivity by accelerating the generation of devices and common analog structures. All cells are generated at a consistently high level of quality. Silicon quality, yield, silicon performance, and matching are as good as the best full custom layout engineer could produce and well above current fully automated layout generation. Design standards are the same for different designers and different projects. Re–targeting to new technology nodes is effortless.

Find out how HiPer DevGen can accelerate your analog layout design.
Contact us at **AnalogLayout@tannereda.com** to schedule your evaluation.

About Tanner EDA

Tanner EDA provides of a complete line of software solutions that catalyze innovation for the design, layout and verification of analog and mixed-signal (A/MS) integrated circuits (ICs). Customers are creating breakthrough applications in areas such as power management, displays and imaging, automotive, consumer electronics, life sciences, and RF devices. A low learning curve, high interoperability, and a powerful user interface improve design team productivity and enable a low total cost of ownership (TCO). Capability and performance are matched by low support requirements and high support capability as well as an ecosystem of partners that bring advanced capabilities to A/MS designs.

Founded in 1988, Tanner EDA solutions deliver the right mixture of features, functionality and usability. The company has shipped over 33,000 licenses of its software to more than 5,000 customers in 67 countries.

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